Sierra Components, Inc.

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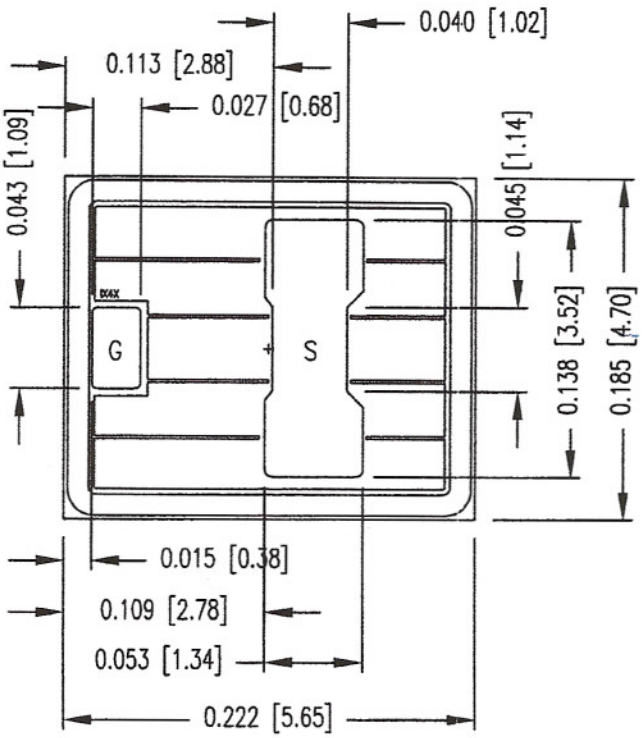
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



NOTE:

1. DIE THICKNESS – 300 ± 25 um [0.012 ± 0.001"]
2. TOP BONDING PAD METAL – 3 um NOMINAL THICK ALUMINUM
3. BACK METAL – 3 LAYERS OF Ti, Ni & Au 1500Å NOMINAL THICK GOLD
4. DIE SIZE TOLERANCE – ±25 um [0.001"]
5. G = GATE
   S = SOURCE (EMITTER FOR IGBT)
   D = DRAIN (COLLECTOR FOR IGBT)
   (Bottom side of die)

APPROVED BY: MG	**DIE SIZE : 0.222 x 0.185 in.**	**DATE: 2/1/11**
MFG: IXYS	**THICKNESS: 0.012 in.**	**P/N: IXGD30N60B2**